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Claims 32 and 36 have been amended to include the subject matter which is identified as "the primary reason for allowance of claims 28-31 and claims 42-45". Namely, each of these claims now recites the fact that a cylindrical opening is etched in the semiconductor which extends below the second opening. Thus, in claim 32 the sixth step provides for dividing the first conductive film by etching the film below a mask pattern, until the first conductive film is divided in the first opening, above the isolation structure and then, simultaneously forming a recess in the second opening.

As pointed out in the reasons for allowance, the references when combined do not disclose these features.

Withdrawal of the rejection of claim 5, dependent on claim 32 is requested in that claim 35 carries all the foregoing limitations of amended claim 32.

Withdrawal of the rejection of claims 38 and 39 under 35 U.S.C. §103 as being unpatentable over Komori et al. (U.S. Pat. 5,300,802) in view of Wolf et al., is requested. Claims 38, and therefore dependent claim 39, now carry the limitations which were noted in the reasons for allowance as being not disclosed by the cited references. Namely, the claims have been amended to more clearly indicate that a cylindrical hole extends through the first conductive film, below the second opening, wherein the first conductive film is etched and insulating layer is exposed in the first opening. Accordingly, these claims are considered to be allowable.

As claims 39, 40 and 41 depend from claim 38, and carry all the limitations thereto and are deemed to allowable as well.

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The undersigned has attempted to amend the remaining rejected claims so that they include all the subject matter which was noted in the reasons for allowance as rendering the application allowable. In the event that any further cooperation with the undersigned is necessary in order to expedite prosecution of this matter, the Examiner is urged to contact him at the telephone number below.

Dated: May 6, 2003

Respectfully submitted,

By _____

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MARKED-UP REVISIONS

IN THE CLAIMS:

32. (Amended) A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming a gate insulating film and a gate electrode in said element active region;

the third step of doping an impurity into said active region of said substrate to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said gate electrode;

the fourth step of forming a first conductive film electrically connected to one of said impurity diffusion layers;

the fifth step of forming a mask pattern having at least first and second openings on said first conductive film;

the sixth step of etching said first conductive film by using said mask pattern as a mask until said first opening divides said first conductive film in said first opening below said second opening above said isolation structure, and simultaneously forms a recess in said second opening having said first conductive film forming a bottom of said recess;

the seventh step of forming a dielectric film so as to cover a surface of said first conductive film; and

the eighth step of forming a second conductive film on said dielectric film opposing said first conductive film through said dielectric film.

36. (Amended) A method of fabricating a semiconductor device, comprising:

the first step of forming a first conductive film in an insulating film region on a semiconductor substrate;

the second step of forming a mask pattern having two openings of different dimensions on said first conductive film;

the third step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film conforming to a shape of one of said openings so as to reach said insulating film region, [thereby] forming a cylindrical hole below said second opening in which a surface of said insulating film region is exposed, and simultaneously forming at least one recess in a surface of said divided first conductive film conforming to a shape of the other opening;

the fourth step of forming an insulating film so as to cover a surface of said first conductive film; and

the fifth step of forming a second conductive film so as to cover a surface of said insulating film opposing said first conductive film through said insulating film.

38. (Amended) A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming an insulating film on said semiconductor substrate in said element active region;

the third step of forming a first conductive film on an entire surface including said insulating film and said element isolation structure;

the fourth step of forming a mask pattern having at least first and second openings on said first conductive film;

the fifth step of etching said first conductive film until said element isolation structure is exposed in said first and second openings by using said mask pattern as a mask, thereby dividing said first conductive film below said first opening, and simultaneously forming a cylindrical hole extending through said first conductive film

below said second opening and said first conductive film is etched until said insulating layer is exposed in said first opening;

the sixth step of forming a dielectric film so as to cover said first conductive film; and

the seventh step of forming a second conductive film on said dielectric film and opposing said first conductive film through said dielectric film.